

A Review Report on XOR-Free Approach for Implementation of Convolutional Encoder

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Abstract – This paper presents a new algorithmic rule to construct an XOR-Free design of a power efficient Convolutional Encoder. Optimisation of XOR operators is the main concern while implementing polynomials over GF that consumes a significant quantity of dynamic power. The projected approach completely removes the XOR-processing operation of a chosen non-systematic, reduces the logical operators and feed-forward generator polynomial, thereby the encoding cost. Implementation of the projected design uses read-only storage (ROM) with pre-processed addressing operations to reduce read-only memory size by about five hundredth. The outcomes of the new architecture reduce the dynamic power up to 21.4% and value up to fifteen with lesser design complexity as compared to standard technique. Due to the excellent error control performance in many communication systems Convolution encoder and Viterbi decoder are widely used. In coding techniques the number of symbols in the source encoded message is increased in a controlled manner in order to facilitate 2 basic demand at the receiver one is Error detection and other is Error correction. Coding could be a technique where redundancy is added to original bit sequence to extend the reliability of the communication. This paper presents a review on implementation of power efficient architecture of Convolution Encoder.

Keywords: Field-programmable gate array (FPGA), Convolutional codes, Forward error correction, and Common sub expression elimination,

I. Introduction

Data transmission dependability and stringent QoS are two main needs of modern 3GPP and 3GPP2 standards over unreliable wireless channels. These standards require to develop and innovate efficient, cost effective forward error correction (FEC) codes for the mobile instrumentation [1][2]. Among the conventional FECs, the Convolutional codes are usually preferred over Block codes because of its economical soft decoding capability and inherent higher coding gain [3]. The error correction capabilities of such codes depend on its Constraint length (K) and maximum free distance (d_{free}) [4]. The key operation of convolution is multiplication, which is implemented using shifts and add. Usually multiple addition operations, increase complexity and consumes a significant amount of dynamic power [5]–[7]. Hence the mitigation of such complexities by reducing the number of logical operators is the prime focus within the encoder design. Common sub expression elimination (CSE) methods have been used to eliminate such redundant computation using the most common bit pattern to optimize the XOR count [8], [9]. This letter proposes a novel algorithmic approach that finds an XOR-Free

processing architecture for nonsystematic, feed-forward Convolutional encoder polynomial represented over GF(2). However, some concatenated codes such as turbo code demands systematic and feedback generator polynomial over GF(2). In this letter effective implementation of nonrecursive convolutional codes is focused. The approach completely replaces modulo-2 based realization of a standard GF(2) based polynomial into a ROM with parity bits as its elements. The ROM based architecture provides ease in FPGA implementation with an additional feature of dynamic reconfiguration. The algorithm is successfully applied with different code rate and constraint length for CDMA2000, WCDMA and the other wireless standards. The Algorithm description, its implementation and outcome of the results are presented in the following subsections.

I.1. Convolution Code (CC)

In Non Line of Sight (NLOS) Communication such as Mobile Wi-Max of CDMA part, the CC is the only required coding scheme. Its computations depend not only on the existing set of input symbols it also

depends up on some of the previous used input symbols. A lattice description is used for convolution encoding that show relation how each possible input to the encoder impacts on the output in shift register. Viterbi algorithms used for decoding. In communication, a convolution code is a type of error-correcting code in which Each m-bit information symbol (each m-bit string) to be encoded is transformed into an n-bit symbol, where m/n is the code rate (n m).

The transformation is a function of the last information symbols, where k is the constraint length of the code.

The convolutional codes are defined by three parameters which are as follow:

(a) Rate: Ratio of the number of input bits to the number of output bits. In this example, rate is 1/2 which means there are two output bits for each input bit.

(b) Constraint length: The number of delay elements in the convolution coding for example with $k = 3$, there are two delaying elements.

(c) Generator polynomial: Wiring of the input sequence with the delay elements to form the output. For example, generator polynomial is $[7,5]_8 = [111,101]_2$. The output from the 78 = 1112 arm uses the XOR of the current input, previous input and the previous to previous input. The output from 58 = 1012 uses the XOR of the current input and the previous to previous input.

$$\text{Rate} = \frac{1}{2}$$

$$\text{Constrain length, } k=3$$

Generator polynomial is $[7, 5]_8 = [111,101]_2$.

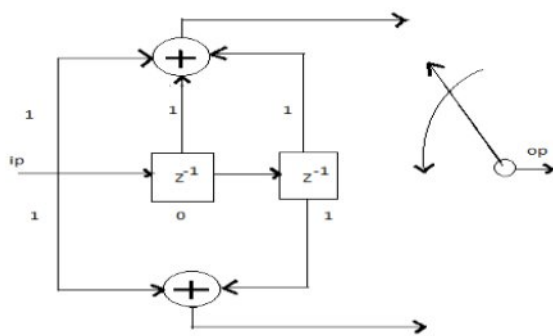


Fig. 1: Convolutional code with Rate 1/2, K=3, Generator Polynomial octal

II. Literature Survey

The G. Purohit, et. al. [1] “A New XOR-Free Approach for Implementation of Convolutional Encoder” In this projected work a brand new algorithmic rule to construct an XOR-Free architecture of an influence efficient Convolutional Encoder. Optimisation of XOR operators is that the main concern whereas implementing polynomials over GF(2), that consumes a significant quantity of dynamic power. The projected approach

utterly removes the XOR-processing operation of a selected non systematic, feed-forward generator polynomial and reduces the logical operators, thereby the encoding value. Hardware (HW) implementation of the projected design uses ROM (ROM) with pre processed addressing operations to reduce read-only memory size by nearly five hundredth. The results of the new architecture reduce the dynamic power up to 21.4% and HW cost up to 15% with lesser design complexity as compared to conventional method. The Hardware co simulation of the architecture is first validated and then implemented with Xilinx Virtex-V FPGA. The problem of optimization of modulo-2 adder and proposes a novel algorithm to implement XOR-Free architecture for Convolutional Encoder. The approach reduces the standard polynomial into a ROM and eases the FPGA implementation. The architecture is successfully tested for 3GPP and 3GPP2 wireless standards.

Rupesh S. Shelar et. Al [2] “Decomposition of Finite State Machines for Area, Delay Minimization”, in this paper described a technique for the decomposition of an N state machine into two interacting pN state machines. We observe that an effective implementation of the original machine can be obtained by one-hot implementations of the two smaller interacting machines, especially when the size of original state machine is large. Based on an empirical study, we observe that decomposition followed by one-hot implementations of the constituent machines can be superior to conventional state assignment tools when area effective and high performance implementations of large state machines are desired. Especially in the case of delays, our results are almost always significantly better than those obtained using conventional state assignment tools

Joachim Hagenauer et.al. [3] “Forward error correcting for CDMA systems” In this proposed work the technique or principle is based on Spread spectrum systems, forward error correcting (FEC) methods is applied in specially code division multiple access systems (CDMA). In fact, almost all CDMA systems use one or the other way of FEC. Author covering some aspect of FEC channel coding in CDMA system: CDMA/FEC system viewed as concatenated schemes with inner and outer decoding. And how such a system can be improved by using a soft-in/soft-out decoder which passes a soft decision from the inner to the outer decoder. Further improvement is gained by using another soft-in/soft- out decoder for the outer code.

Khader Mohammad et. Al [4] “Efficient FPGA implementation of convolution”, in this paper presented an optimized implementation of discrete linear convolution. This particular model has the advantage of being finetuned for signal processing; in this case it uses the mean squared error measurement and objective measures of enhancement to achieve a more effective signal processing model. This implementation has the

advantage of being optimized based on operation, power and area. To accurately analyse our proposed system, we have coded our design using the Verilog hardware description language and have synthesized it for FPGA products using ISE, Modelsim and DC compiler for other processor usage. Second, we implemented an illustrative example 4X4 convolver. Similarly, the presented concept can be extended on an NXN case. The functionality of the convolver was tested and verified successfully on a XILINIX SE FPGA and design compiler. The proposed circuit uses only 5mw and saves almost 35% area and it takes 20ns to complete. This shows improvement of more than 50% less power. As FPGA technology matures and much larger arrays become practical, techniques that allow the automatic generation of highly parallel architectures will become central to high performance computing. We have described some simple techniques for generation of convolution pipelines for image processing and other applications. Higher level techniques and approaches are

John Dielissen et.al. [5] “Multi standard FEC Decoders for Wireless Devices” In this proposed work is based on the compression of the era of mobile terminal the real-time support of multiple/different transmission standards. Forward error correction decoding functionality is including in some of these standards. Author review the options for the arrangements of common decoder families (Reed–Solomon, Viterbi, Turbo and low-density parity check) within same hardware platform. That although desired combinations may result in silicon area saving, in general cases the reuse possibilities are limited to much less than the overall decoder area. Due to the need of handy and fast processing area reduction and low power consuming devices are widely used.

III. Method

III.1. Convolution Encoder

Please In this encoder, data bits are provided at a rate of k bits per second. Channel symbols are output at a rate of $n = 2k$ symbols per second. The input bit is stable during the encoder cycle. The encoder cycle starts when an input clock edge occurs. When the input clock edge occurs, the output of the left-hand flip-flop is clocked into the right-hand flip-flop, the previous input bit is clocked into the left-hand flip-flop, and a new input bit becomes available. Then the outputs of the upper and lower modulo-two adders become stable. The output selector (SEL A/B block) cycles through two states-in the first state, it selects and outputs the output of the upper modulo-two adder; in the second state, it selects and outputs the output of the lower modulo-two adder.

The encoder shown above encodes the $K = 3, (7, 5)$ convolutional code. The octal numbers 7 and 5 represent the code generator polynomials, which when read in binary (111_2 and 101_2) correspond to the shift register

connections to the upper and lower modulo-two adders, respectively. This code has been determined to be the "best" code for rate $1/2, K = 3$. It is the code I will use for the remaining discussion and examples, for reasons that will become readily apparent when we get into the Viterbi decoder algorithm.

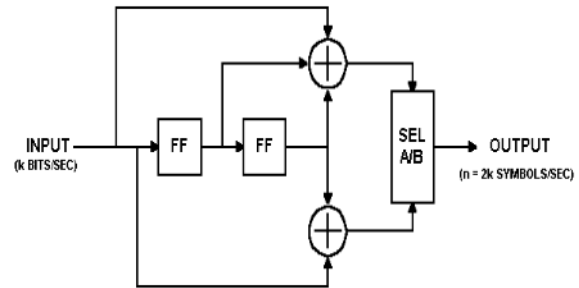


Fig.2: Convolution Encoder

III.2. Serial/Parallel Multiplier

The general architecture of the serial/parallel multiplier is shown in the figure below. One operand is fed to the circuit in parallel while the other is serial. N partial products are formed each cycle. On successive cycles, each cycle does the addition of one column of the multiplication table of $M \times N$ PPs. The final results are stored in the output register after $N+M$ cycles. While the area required is $N-1$ for $M=N$.

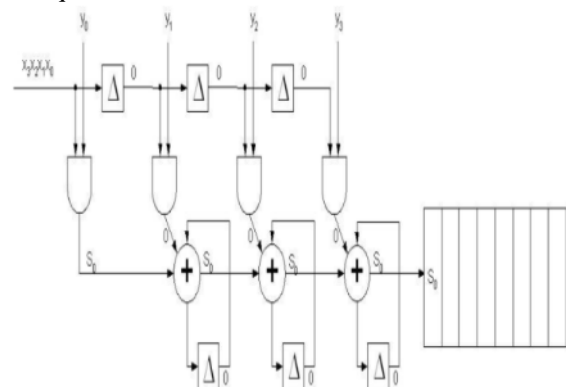


Fig. 3. Serial & parallel multiplier

IV. Conclusion

The Proposed system is improve of modulo-2 adders that are a big source of dynamic power and proposes a novel algorithm to implement XOR-FREE design for non-systematic, feed forward convolution encoder. The approach reduces the standard polynomial into a ROM and eases the FPGA implementation. Proposed method is perform all XOR- Free operation and use minimum LUT and FF.

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